IN THE CLAIMS:

Please cancel claims 1-13 without prejudice to disclaimer of the subject matter as cited therein.

Please add new claims 14-26 as follows.

LISTING OF CURRENT CLAIMS

Claim 14. (new) A circuit providing a stable timing clock comprising:

a) an antenna inducing an AC voltage;

b) an AC/DC rectifier electrically connected to the antenna;

c) a filter electrically connected to the AC/DC rectifier;

d) a voltage limiter electrically connected to the filter, the AC/DC rectifier, the filter and the voltage limiter converting the AC voltage into a first DC voltage;

e) a step-down clamping circuit electrically connected to the voltage limiter and converting the first DC voltage into a second DC voltage;

f) an oscillating circuit electrically connected to the step-down clamping circuit and utilizing the second DC voltage as an operating voltage, the oscillating circuit generating a first timing clock signal having a voltage potential lower than a voltage potential of the second DC voltage; and

g) a voltage potential-converting circuit electrically connected to the oscillating circuit and converting the first timing clock signal into a second timing clock signal having a voltage potential higher than a voltage potential of the first timing clock signal,

wherein the second timing clock signal is produced from the AC voltage incuced by the antenna.

Claim 15. (new) The circuit according to claim 14, wherein the first DC voltage having rippling wave and voltage potential having variations larger than the second DC voltage.

Claim 16. (new) The circuit according to claim 14, wherein the second DC voltage is a preferred DC voltage.

Claim 17. (new) The circuit according to claim 14, wherein the second DC voltage is smaller than the first DC voltage.

Claim 18. (new) The circuit according to claim 14, wherein the step-down clamping circuit includes a resistance, a capacitance, and a clamping circuit.

Claim 19. (new) The circuit according to claim 18, wherein the clamping circuit includes a P-type metal oxide semiconductor and a N-type metal oxide semiconductor.

Claim 20. (new) A circuit providing a stable timing clock comprising:

a) an antenna inducing an AC voltage;

b) a rectifying circuit electrically connected to the antenna and converting the AC voltage into a first DC voltage;

c) a step-down clamping circuit electrically connected to the voltage limiter and converting the first DC voltage into a second DC voltage;

d) an oscillating circuit electrically connected to the step-down clamping circuit and utilizing the second DC voltage as an operating voltage and generating a first timing clock signal having a voltage potential lower than a voltage potential of the second DC voltage; and

e) a voltage potential-converting circuit electrically connected to the oscillating circuit and converting the first timing clock signal into a second timing clock signal having a voltage potential higher than a voltage potential of the first timing clock signal,

wherein the second timing clock signal is produced from the AC voltage induced by the antenna.

21. (new) The circuit according to claim 20, wherein the rectifying circuit having a AC/DC rectifier, a filter, and a voltage limiter.

22. (new) The circuit according to claim 20, wherein the first DC voltage having rippling wave and voltage potential having variations larger than the second DC voltage.

23. (new) The circuit according to claim 20, wherein the second DC voltage is a preferred DC voltage.

24. (new) The circuit according to claim 20, wherein the second DC voltage is smaller than the first DC voltage.

25. (new) The circuit according to claim 20, wherein the step-down clamping circuit includes a resistance, a capacitance, and a clamping circuit.

26. (new) The circuit according to claim 25, wherein the clamping circuit includes a P-type metal oxide semiconductor and a N-type metal oxide semiconductor.